IN THE CLAIMS:

Please cancel claims 1-21, without prejudice and add new claims 22-40 as follows:

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22. (New) A CMOS basic cell comprising:

an N-channel transistor and a P-channel transistor on a semiconductor substrate; and

an interconnect pattern which is electrically isolated and which exists between said N-channel transistor and said P-channel transistor,

wherein said interconnect pattern is formed in an uppermost interconnect layer of said CMOS basic cell.

23. (New) The CMQS basic cell of Claim 1, wherein said interconnect pattern extending either along a perpendicular direction or along a horizontal direction relative to a boundary between said N-channel transistor and said P-channel transistor.

24. (New) The CMOS basic cell of Claims 22 or 23 further comprising: a power supply pattern, a master pattern and another interconnect pattern different from said interconnect pattern,

wherein said another interconnect pattern exists between said N-channel

transistor and said master pattern, said another interconnect pattern extending either along a perpendicular direction or along a horizontal direction relative to a boundary between said N-channel transistor and P-channel transistor, said another interconnect pattern electrically disconnected from said N-channel transistor and said P-channel transistor and formed in an uppermost interconnect layer.

25. (New) The CMOS basis cell of any one of Claims 22 to 24, wherein said interconnect pattern is mutually connected electrically with an interconnect pattern of another CMOS basic cell, when said CMOS basic cell is adjacent to said another CMOS basic cell.

26. (New) The gate array semiconductor integrated circuit of any one of Claims 22 to 25, wherein two or more said CMOS basic cells are electrically connected by a higher interconnect pattern located in a layer that is higher than said interconnect pattern.

27. (New) The gate array semiconductor integrated circuit according to Claim 26, wherein said higher interconnect pattern is located in a region between said P-channel transistors and said N-channel transistors except the both ends of said interconnect pattern, and

wherein said interconnect pattern which intersects said higher interconnect pattern is electrically connected with a higher interconnect pattern except said higher interconnect pattern which intersects said interconnect pattern.

28. (New) A method for fabricating a gate array semiconductor integrated circuit including a plurality of basic cells and a higher interconnect pattern provided above said basic cells, comprising the steps of:

arranging a plurality of CMOS basic cells according to any one of Claims 22 to 26 on a semiconductor substrate; and

realizing a logic circuit including a clock signal line by using said interconnect patterns formed in the uppermost interconnect layers of said CMOS basic cells and said higher interconnect pattern.

29. (New) A method for fabricating a gate array semiconductor integrated circuit including a plurality of basic cells and a higher interconnect pattern provided above said basic cells, comprising the steps of:

arranging a plurality of CMOS basic cells according to one of Claims 22 to 26 on a semiconductor substrate; and

realizing a logic circuit including transistors connected to each other in parallel by

using said interconnect patterns formed in the uppermost interconnect layers of said CMOS basic cells and said higher interconnect pattern.

30. (New) A method for fabricating a gate array semiconductor integrated circuit including a plurality of basic cells and a higher interconnect pattern provided above said basic cells, comprising the steps of:

arranging a plurality of CMOS basic cells according to one of Claims 22 to 26 on a semiconductor substrate; and

realizing a composite logic circuit by using said interconnect patterns formed in the uppermost interconnect layers of said CMOS basic cells and said higher interconnect pattern.

31. (New) A method for fabricating a gate array semiconductor integrated circuit including a plurality of basic cells and a higher interconnect pattern provided above said basic cells, comprising the steps of:

arranging a plurality of CMOS basic cells according to Claims 22 to 26 on a semiconductor substrate; and

realizing a logic circuit including a control signal line by using said interconnect patterns formed in the uppermost interconnect layers of said CMOS basic cells and said higher interconnect pattern.

32. (New) A method for fabricating a gate array semiconductor integrated circuit including a plurality of basic cells and a higher interconnect pattern provided above said basic cells, comprising the steps of:

arranging a plurality of CMOS basic cells according to one of Claims 22 to 26 on a semiconductor substrate; and

realizing a logic circuit for a memory by using said interconnect patterns formed in the uppermost interconnect layers of said CMOS basic cells and said higher interconnect pattern.

33. (New) A method for fabricating a gate array semiconductor integrated circuit including a plurality of basic cells and a higher interconnect pattern provided above said basic cells, comprising the steps of:

arranging a plurality of CMOS basic cells according to one of Claims 22 to 26 on a semiconductor substrate; and

realizing a flip-flop circuit having a scan test function by using said interconnect patterns formed in the uppermost interconnect layers of said CMOS basic cells and said higher interconnect pattern.

34. (New) A CMOS basic cell comprising:

an N-channel transistor and a P-channel transistor existing on a semiconductor substrate, said CMOS basic cell being electrical coupled with other adjacent CMOS basic cells;

wherein a gate of at least one of said N-channel transistor and said P-channel transistor has a hooked shape including a first bent part bending in one sideward direction at an upper portion thereof and a second bent part bending in an opposite sideward direction at a lower portion thereof, and

a diffusion region of at least one of said N-channel transistor and said P-channel transistor having a hooked shape having a first bent part bending in one sideward direction at an upper portion thereof and a second bent part bending in an opposite sideward direction at a lower portion thereof,

said upper portion of said gate is bent oppositely to said upper portion of said diffusion region.

35. (New) The CMOS basic cell of Claim 34, wherein a first N-channel transistor and a first P-channel transistor are formed to extend along a vertical direction, and

a second N-channel transistor is disposed on a side of said first N-channel transistor and a second P-channel transistor is disposed on a side of said first P-channel transistor, and

a gate of each of said first and second N-channel transistors and said first and second

P-channel transistors is formed in the hooked shape.

36. (New) The CMOS basic cell of Claim 35, wherein the gates of said first and second N-channel transistors are disposed in a manner that said first bent part of one gate overlaps said second bent part of the other gate when viewed along the vertical direction from one position in a horizontal direction, and

the gates of said first and second P-channel transistors are disposed in a manner that said first bent part of one gate overlaps said second part of the other gate when viewed along the vertical direction from one position in the horizontal direction.

37. (New) The CMOS basic cell of Claim 35, wherein said first and second N-channel transistors share one diffusion region and said first and second P-channel transistors share one diffusion region,

each of said diffusion regions is divided into a shared diffusion region shared by said first and second N-channel or P-channel transistors and positioned between the gates of said first and second N-channel or P-channel transistors; a first dedicated diffusion region positioned on a side of said gate of said first N-channel or P-channel transistor opposite to said shared diffusion region; and a second dedicated diffusion region positioned on a side of said gate of said second N-channel or P-channel transistor opposite to said shared diffusion region,

said first bent part is formed in said first dedicated diffusion region, and

said second bent part is formed in said second dedicated diffusion region.

38. (New) The CMOS basic cell according to any one of Claims 34 to 37, comprising, outside of a transistor region where said N-channel transistor are disposed, a fixed interconnect region where a power supply interconnect and a ground interconnect are disposed.

39. (New) The CMOS basic cell according to any one of Claims 34 to 37, said first bent part of said gate of said P-channel transistor and said first bent part of said diffusion region of said P-channel transistor of another CMOS basic cell is electrically connected with said higher interconnect pattern,

wherein said higher interconnect pattern extends along a horizontal direction to the perpendicular from said N-channel transistor to said P-channel transistor.

40. (New) A method for fabricating a gate array semiconductor integrated circuit including a plurality of basic cells arranged in a horizontal direction, comprising a step of arranging a plurality of CMOS basic cells according to any one of Claims 34 to 37 in the horizontal direction in a manner that said first bent part of one CMOS basic cell overlaps said second bent part of another adjacent CMOS basic cell when viewed